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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,774	09/17/2003	Kyoung Mook Lee	8733.915.00-US	1766

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EXAMINER	
NGUYEN, DUNG T	

ART UNIT	PAPER NUMBER
2871	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,774	LEE ET AL.	
	Examiner	Art Unit	
	Dung Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-8, 10-15, 17-25 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., WO 03/058332 A1, in view of Baek, US 6,256,077.

Regarding claims 1, 3-8, 10-15, 17-25, 27-30, Lee et al. disclose a an array substrate (figure 3) for a liquid crystal display (LCD) device comprising:

. a substrate 100;

. a plurality of gate lines 135;

. a plurality of thin film transistors TFTs 195, each having a gate electrode 110, a source/drain electrode 140/145;

. an interlayer insulating layer 155;

. a first gate redundancy line 170;

. a passivation layer 180;

. a second gate redundancy line 175;

. a pixel electrode (185);

Lee et al., however, do not disclose the first gate redundancy line being formed of the same material as one of the source and the drain electrode. Baek does disclose the gate pad can be formed by chrome material (col. 6, ln 52). Therefore, it would have been obvious to one skilled in the art at the time of the invention was mad to form a gate redundancy electrode and source/drain electrode having a same based material (e.g., chrome), since it is a common practice in the art to simplify process steps for forming an LCD device (see abstract).

3. Claims 2, 9, 16 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., WO 03/058332 A1, in view of Baek, US 6,256,077, further in view of Kitakado et al., US 6,461,899.

Regarding claims 2, 9, 16 and 26, although Lee et al. do not explicitly disclose a top gate type TFT using in the LCD device, Kitakado et al. do disclose top gate type and bottom gate type structure is known structures for a TFT manufactured on a glass substrate (col. 1, lines 55-57). Therefore, it would have been an obvious to one having ordinary skill in the art at the time the invention was made to employ the Lee et al device having a top gate TFT since the examiner takes Office Notice of the equivalence of a top gate type TFT and a bottom type TFT for their use in the display art and the selection of any of these known equivalents to operate a display device would be within the level of ordinary skill in the art.

Response to Arguments

Applicants' arguments are as follow:

a. the Lee's reference numbers 170 and 175 refer to gate pad electrode and pad contact hole rather than a first/second gate redundancy lines.

b. a gate pad electrode exits on the periphery of a device while Applicant's gate redundancy line are formed internal to the device and not on the periphery of the device.

c. the Examiner did not address the limitation of " a first gate redundancy line formed on the interlayer insulating layer, and connected electrically with just one of gate electrodes, ..., through a first gate contact hole".

d. Lee does not disclose the first gate redundancy line being formed of the same material as one of the source and the drain electrode.

e. the Examiner did not address the limitation of "a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer".

f. Applicants notes that top gate and bottom gate TFT are manufactured by very different processes and the method claims are not just device limitations but require a manner of formation.

The Examiner's responses are as follow:

a. Examiner notes that Applicants fail to establish any special definition of "gate redundancy line". Therefore, for the examination purposes, the "gate redundancy line" is consider as of any wire formed on the interlayer insulating layer and connected to the gate electrode as claimed. In particular, the Lee's gate pad formed over the insulating layer 155 and inherently connected to the gate electrode through the gate line (see figure 3). In other words, the gate pad can be considered as a gate redundancy line as claimed as well.

b. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., gate redundancy line are formed internal to the device and not on the periphery of the device) are not

recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

c. it should be noted that the limitations of a first gate redundancy line (gate pad 170) formed on the interlayer insulating layer (155), and connected electrically with just one of gate electrodes (connected to the TFT through a gate electrode), ..., through a first gate contact hole (gate pad hole 165) is clearly shown in the Lee's figures 3 and 4B. In addition, one of ordinary skill in the art would be able to merely find how the gate pad contacted to the TFT through the contact hole; so as, needless to address each single element while it is known in the art.

d. Applicant argues that the office action fails to set forth a prima facie case of obviousness and seasonably challenges the Examiner's using an Official Notice for "first gate redundancy line being formed of the same material as one of the source and the drain electrode". Accordingly, the Examiner provides herewith evidence to support the Office's position and § 103 rejection as stated above (Baek '077).

e. as same as part c, Lee clearly discloses the limitation of a pixel electrode 190 electrically connected with the drain electrode 145 through the drain contact hole 185 formed in the passivation layer 180 (see figure 4A).

f. the Examiner agrees that top gate and bottom gate TFT might be manufactured by very different processes; however, the specific step(s) of manufacturing the top gate and/or bottom gate TFT is not yet recited in claim. In other words, absent any showing of criticality, the recited limitation "top gate" or "bottom gate" would have been obvious to one skilled in the art to

modify the Lee's display by using top gate and/or bottom gate since it is a known structure for driving LCD display as evidence from

Kitakado et al ('899).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung Nguyen whose telephone number is 571-272-2297. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DN
10/01/2007

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